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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,861	03/16/2004	Hiroki Nakamura	250442US2	1575

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EXAMINER	
SEMENENKO, YURIY	

ART UNIT	PAPER NUMBER
2841	

NOTIFICATION DATE	DELIVERY MODE
11/27/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/800,861	NAKAMURA, HIROKI	
	Examiner	Art Unit	
	Yuriy Semenenko	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *0316/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/14/2007 has been entered.

Response to Amendment

2. Amendment filed on 08/21/2007 has been entered.
In response to the Office Action dated 05/21/2007, Applicants have cancelled claims 1-29. Claims 30-38 are newly added.
Claims 30-38 are now pending in the application.

Claim Objections

3. Claim 35 objected to because of the following informalities:
line 3; It should be –an insulating substrate; -

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make

and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 31, 32 and 33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is not any information about a third metal diffusion-preventing layer formed on the source region and the drain region; a copper wiring layer formed on the third metal diffusion-preventing layer; and a fourth metal diffusion-preventing layer formed to surround the copper wiring layer, as claimed in claim 31, a fifth metal diffusion-preventing layer which is provided on one of the substrate and a sixth metal diffusion-preventing layer, as claimed in claim 32 in specification.
Claim 33 depends on claim 32 and has same deficiency.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 37 and 38 are rejected under 35 U.S.C. 102(a) as being anticipated by Yamazaki et al. (US 6791112) hereinafter Yamazaki.

As to claim 37: Yamazaki discloses in Fig. 1A a thin-film transistor comprising: a source region 105 and a drain region 106 which are provided with an interval on an insulating substrate 101 (glass- column 4, lines 8-14); a gate insulator layer 112 which is provided over the interval between the source region 105 and the drain region 106; a gate electrode 115 which is provided on the gate insulator layer 112; and a source electrode 120 and a drain electrode 121 which are provided on the source region 105 and the drain region 106, respectively, wherein the gate electrode Fig. 17D comprises: a first metal diffusion-preventing layer (silicon nitride -column 19, lines 7-16) formed on the gate insulator layer; a metal layer 1707 formed on the first metal diffusion-preventing layer; and a second metal diffusion-preventing layer (silicon nitride -column 19, lines 7-16) covering the exposed surface including the side surface of the multilayered structure having the metal layer and the first metal diffusion-preventing layer, and wherein the metal layer is surrounded by the first metal diffusion-preventing layer and the second metal diffusion-preventing layer, and has a forward tapered cross section Fig. 18B and (column 20, lines 14-17).

As to claim 38: Yamazaki discloses the thin-film transistor substantially as claimed claim 37, wherein the insulating substrate 101, Fig. 1A is formed of one of glass, a quartz glass, ceramics, and a resin material (glass- column 4, lines 8-14).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6.1. Claims 30 - 35 and 36 are rejected under 35U.S.C. 103(a) as being unpatentable over Yamazaki in view of Ueno et al. (PGPub. No: 2003/0008075) hereinafter Ueno.

As to claim 30: Yamazaki discloses in Fig. 1A a thin-film transistor comprising: a source region 105 and a drain region 106 which are provided with an interval on an insulating substrate 101(glass- column 4, lines 8-14); a gate insulator layer 112 which is provided over the interval between the source region 105 and the drain region 106; a gate electrode 115 which is provided on the gate insulator layer 112; and a source electrode 120 and a drain electrode 121 which are provided on the source region 105 and the drain region 106, respectively, wherein the gate electrode Fig. 17D comprises: a first metal diffusion-preventing layer (silicon nitride -column 19, lines 7-16) formed on the gate insulator layer; a metal layer 1707 formed; and a second metal diffusion-preventing layer (silicon nitride -column 19, lines 7-16) covering the exposed surface including the side surface of the multilayered structure having the metal layer, and wherein the metal layer is surrounded by the first metal diffusion- preventing layer and the second metal diffusion-preventing layer, and have a forward tapered cross section, Fig. 18B and (column 20, lines 14-17).

except Yamazaki does not explicitly teach a metal seed layer formed on the first metal diffusion-preventing layer.

Ueno discloses also discloses in the "Background of the invention" section, at the time the invention was made, it was well know to use a metal seed layer 17, Fig. 1 formed on the first metal diffusion-preventing layer 15; and a metal wiring layer 11 formed on the metal seed layer 17.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Yamazaki to include in his invention that a metal seed layer formed on the first metal diffusion-preventing layer to improve adhesion metal to metal diffusion-preventing layer.

As to claim 31: Yamazaki, as modified, discloses the thin-film transistor having all of the claimed features as discussed above with respect claim 30, wherein the source electrode 122, Fig. 1A and the drain electrode 121 comprises: a third metal diffusion-preventing layer (silicon nitride -column 19, lines 7-16) formed on the source region 110 and the drain region 109; a copper wiring layer 117 formed on the third metal diffusion-preventing layer (silicon nitride -column 19, lines 7-16); and a fourth metal diffusion-preventing layer formed to surround the copper wiring layer 117.

As to claims 32 and 33: Yamazaki, as modified, discloses the thin-film transistor having all of the claimed features as discussed above with respect claim 31, wherein a plurality of the thin-film transistors 500, 506, Fig. 4 are arranged to form a matrix Fig. 4, and the thin-film transistors have scanning lines 402 connected to the gate electrodes of the thin-film transistors 500, 506, and signal lines 403 connected to one of the source electrodes and the drain electrodes of the thin-film transistors, the signal lines being provided such that they are surrounded by the first metal diffusion-preventing layer (silicon nitride -column 19, lines 7-16) and the second metal diffusion-preventing layer; wherein the gate electrode, the source electrode, and the drain electrode each has wiring connected thereto (column 20, Embodiment 11) and metal diffusion-preventing layer (column 20, lines 47-51); a metal wiring layer of forward tapered cross section (Fig. 18B and (column 20, lines 14-17), which is connects one end thereof to any one of the gate electrode, the source electrode (column 26, lines 8-24),

Although Yamazaki does not explicitly teach the wiring comprises: a fifth metal diffusion-preventing layer which is provided on one of the substrate and the insulator layer; a metal seed layer formed on the fifth metal diffusion-preventing layer; a metal wiring layer, which is provided on the metal seed layer; and a sixth metal diffusion-preventing layer covering the exposed surface including the side surface of the multilayered structure having the metal seed layer and the metal wiring layer, and wherein the metal seed layer and the metal wiring layer are surrounded by the first metal diffusion-preventing layer and the second metal diffusion-preventing layer, this is just repeating claim 30 for wiring layer and so it is old and well known how to use it. Yamazaki also teaches that such structure permit variations (column 26, lines 8-10). Further, it has been held in re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960) (Although the reference did not disclose a plurality of ribs, the court held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced.).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Yamazaki to include in his invention that the wiring comprises: a fifth metal diffusion-preventing layer which is provided on one of the substrate and the insulator layer; a metal seed layer formed on the fifth metal diffusion-preventing layer; a metal wiring layer, which is provided on the metal seed layer; and a sixth metal diffusion-preventing layer covering the exposed surface including the side surface of the multilayered structure having the metal seed layer and the metal wiring layer, and wherein the metal seed layer and the metal wiring layer are surrounded by the first metal diffusion-preventing layer and the second metal diffusion-preventing layer in order to improve adhesion metal to metal diffusion-preventing layer.

As to claim 34: Yamazaki, as modified, discloses the thin-film transistor having all of the claimed features as discussed above with respect claim 30, wherein the insulating substrate 101, Fig. 1A is formed of one of glass, a quartz glass, ceramics, and a resin material (glass- column 4, lines 8-14).

As to claim 35: Yamazaki discloses in Fig. 1A a thin-film transistor comprising: a source region 105 and a drain region 106 which are provided with an interval on an insulating substrate 101(glass- column 4, lines 8-14); a gate insulator layer 112 which is provided over the interval between the source region 105 and the drain region 106; a gate electrode 115 which is provided on the gate insulator layer 112; and a source electrode 120 and a drain electrode 121 which are provided on the source region 105 and the drain region 106, respectively, wherein the gate electrode Fig. 17D comprises: a first metal diffusion-preventing layer (silicon nitride -column 19, lines 7-16) formed on the gate insulator layer; a metal layer 1707 having a forward tapered cross section, Fig. 18B and (column 20, lines 14-17); and a second metal diffusion-preventing layer (silicon nitride -column 19, lines 7-16) covering the exposed surface including the side surface of the multilayered structure having the metal layer, and wherein the metal layer is surrounded by the first metal diffusion- preventing layer and the second metal diffusion-preventing layer,

except Yamazaki does not explicitly teach a metal seed layer formed on the first metal diffusion-preventing layer.

Ueno discloses also discloses in the "Background of the invention" section, at the time the invention was made, it was well know to use a metal seed layer 17, Fig. 1 formed on the first metal diffusion-preventing layer 15; and a metal wiring layer 11 formed on the metal seed layer 17.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Yamazaki to include in his invention that a metal seed layer formed on the first metal diffusion-preventing layer to improve adhesion metal to metal diffusion-preventing layer.

As to claim 36: Yamazaki, as modified, discloses the thin-film transistor having all of the claimed features as discussed above with respect claim 35, wherein the insulating substrate 101, Fig. 1A is formed of one of glass, a quartz glass, ceramics, and a resin material (glass- column 4, lines 8-14).

Response to Arguments

7. Applicant's arguments filed on 03/26/2007 are considered and acknowledged but are moot in view of the new ground(s) of rejection. Nevertheless, examiner points out, in response to applicant's arguments against the Ueno's reference, Ueno discloses in the "Background of the invention" section a metal seed layer 17, Fig. 1 formed on the first metal diffusion-preventing layer 15.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego F. F. Gutiérrez can be reached on (571)- 272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YS

IB Parker
[Primary Examiner
AU: 2841